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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,704	10/31/2003	Robert O. Conn	X-1416-3 US	1939

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EXAMINER	
WILLIAMS, ALEXANDER O	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/698,704	CONN, ROBERT O.
	Examiner	Art Unit
	Alexander O. Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 8 and 12 to 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 8 and 12 to 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/3/06 & 8/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS filed 10/31/03*.

Serial Number: 10/698704 Attorney's Docket #: X-1416-3US
Filing Date: 10/31/2003;

Applicant: Conn Examiner: Alexander Williams

Applicant's Amendment filed 1/3/06 to the election of Group I (claims 1 to 8 and 12 to 16) filed 6/29/05 to the species elected of species of figures 1 to 7 filed 4/4/05 has been acknowledged.

Claims 9-11 have been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 8 and 12 to 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moro et al. (U.S. Patent Application Publication # 2002/0088977 A1).

1. Mori et al. (figures 1A to 1B) specifically figure 11 show an assembly, comprising: an integrated circuit die 57 having an array of micro-bumps 58 disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package 64 having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first

pattern and the second pattern are substantially identical patterns; and an interposing structure **62** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, but Moro et al.'s figure 11 fail to explicitly show the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads.

Mori et al. (figures 1A and 1B) discloses the interposer coupling a first micro-bump **(connected to second 4 on top of 1)** in a first position in the array of micro-bumps to a first landing pad **(second 4 on the bottom of 1)** located opposite to the first position and to a second landing pad **(first 4 on the bottom of 1)** in the array of landing pads for the purpose of providing a single input signal into several output signals.

2. The assembly of claim 1, Mori et al. show wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the second landing pad of the integrated circuit package.

3. The assembly of claim 2, Mori et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.

4. The assembly of claim 3, Mori et al. show wherein the interposing structure includes no transistor and no PN junction.

5. The assembly of claim 4, Mori et al. show wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

6. The assembly of claim 5, Mori et al. show wherein the interposing structure includes a layer comprising epoxy and fiberglass.

7. The assembly of claim 5, Mori et al. show wherein the interposing structure includes a bypass capacitor (decoupling capacitor).

8. The assembly of claim 5, Mori et al. show wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

12. Mori et al. (figures 1A to 1B) specifically figure 11 show an assembly, comprising: an integrated circuit die **57** having an array of micro-bumps **58** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **64** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; but Mori et al. fail to explicitly show the means **62** for coupling a first micro-bump in a first position in the array of microbumps to a first landing pad disposed opposed the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

Mori et al. (figures 1A and 1B) discloses the means for coupling a first micro-bump **(connecting to second 4 on the top of 1)** in a first position in the array of microbumps to a first landing pad **(second 4 on the bottom of 1)** disposed opposed the first position and to a second landing pad **(first 4 on the bottom of 1)** located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the

integrated circuit package for the purpose of providing a single input signal into several output signals.

13. The assembly of claim 12, Mori et al. show wherein the means is also for providing a bypass current to the integrated circuit die (decoupling capacitor).

14. The assembly of claim 12, Mori et al. show wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. The assembly of claim 12, Mori et al. show wherein the means has a planar form and is less than 500 microns thick.
Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The assembly of claim 12, Mori et al. show wherein the integrated circuit die is an application specific integrated circuit (ASIC) (inherent).

Therefore, it would have been obvious to one of ordinary skill in the art to use Mori et al.'s interposer of figure 1B to modify Moro et al.'s interposer for the purpose of providing a single input signal into several output signals.

[0025] It is a still further object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

[0027] It is further more object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit

exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor allows a reduction of a total inductance of the capacitor and a wiring.

[0028] It is more over object of the present invention to provide a novel stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor reduces a signal transmission delay.

[0031] It is another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

[0033] It is further another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor allows a reduction of a total inductance of the capacitor and a wiring.

[0034] It is furthermore another object of the present invention to provide a novel method of forming a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor reduces a signal transmission delay.

[0037] It is an additional object of the present invention to provide a novel semiconductor device including a stacked capacitor being placed as an interposer between a circuit board and a large scale integrated circuit exhibiting a high speed performance, wherein the stacked capacitor serves as a decoupling capacitor for compensating a voltage drop upon variation in load of the large scale integrated circuit, and the stacked capacitor has a high capacity for a unit packaging area.

TWELFTH EMBODIMENT

[0119] A twelfth embodiment according to the present invention will be described with reference to the drawings. FIG. 11 is a cross sectional elevation view of a semiconductor device over a circuit board in a twelfth embodiment according to the present invention. A stacked capacitor 62 is provided as an interposer between a printed circuit board 64 and a large scale integrated circuit bare chip 57. The stacked capacitor 62 is electrically connected to the large scale integrated circuit bare chip 57 through first, second and third terminal electrodes 59, 60, and 61 and solder bumps 58. The stacked capacitor 62 is also electrically connected to the printed circuit board 64 through the first, second and third terminal electrodes 59, 60, and 61 and the solder bumps 58. The first terminal electrode 59 is connected to the signal line of the large scale integrated circuit. The second terminal electrode 60 is connected to the power line. The third terminal electrode 61 is connected to the ground line.

Claims 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Moro et al. (U.S. Patent Application Publication # 2002/0088977 A1) in view of Berlin et al. (U.S. Patent # 6,104,082).

Moro et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the integrated circuit die is an application specific integrated circuit (ASIC).

Berlin et al. show a metallization structure for altering connections. Specifically, Berlin et al. (figures 1 to 13b) specifically figure 2b discloses an assembly, comprising: an integrated circuit die (chips 1-6) having an array of micro-bumps **62** disposed on a surface of the integrated circuit die in a first pattern; an integrated circuit package **68** having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern, wherein the first pattern and the second pattern are substantially identical patterns; and an interposing structure **60'** disposed inside the integrated circuit package between the integrated circuit die and the inside surface of

the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed in a different position in the array of landing pads, wherein the integrated circuit die **(chips 1-6)** is an application specific integrated circuit (ASIC) for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

(32) The tailorable metallization of the present invention also provides a scheme for rapidly creating or altering circuit configurations; in essence application specific integrated circuits are quickly fabricated by selecting and deselecting circuits with the metallization tailoring methods disclosed herein. While it would be advantageous to test circuit elements first to ensure the functionality of the included circuits before finalizing the metallization, these ASIC circuits could also be built with the tailorable wiring of the present invention without the intermediate test. The wiring can be tailored by methods such as opening fuses, providing ribbon connections, providing bump connections, or providing photolithographically formed shapes as described herein above. In this case, defective circuits would be included and would result in yield loss but other functional chips would be fabricated in much less time than would be required to provide masks.

Therefore, it would have been obvious to one of ordinary skill in the art to use Berlin et al.'s ASIC chip type to modify Moro et al.'s chip for the purpose of providing an electronic module that permits changing connections while retaining a constant interface to the electronic module.

Response

Applicant's arguments filed 1/3/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 12" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/653,758,774,778,737,738,734,686,685,723,691,774,692,693 361/306.3,312,313,321.1,321.4	9/11/05 4/13/06
Other Documentation: foreign patents and literature in 257/653,758,774,778,737,738,734,686,685,723,691,774,692,693 361/306.3,312,313,321.1,321.4	9/11/05 4/13/06
Electronic data base(s): U.S. Patents EAST	9/11/05 4/13/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/13/06